IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Steve M. Danziger, et al.**

Serial No.: **TO BE ASSIGNED** Art Unit: **TO BE ASSIGNED**
Divisional of 09/321,565

Filed: **April 12, 2001** Examiner: **TO BE ASSIGNED**

For: **Method and Apparatus for Evaluating a Known Good Die Using Both Wire Bond and Flip-Chip Interconnects**

PRELIMINARY AMENDMENT

Assistant Commissioner of
Patent and Trademarks
Washington, D.C. 20231
BOX: PATENT APPLICATIONS

Sir:

This application is a divisional application of serial number 09/321, 565. After assigning a serial number to the above-captioned application and before calculating the fee, please undertake the following changes:

IN THE SPECIFICATION:

Please amend the specification as follows:

Please insert the following paragraph at line 3 of page 1:

---This application is a divisional of U.S. patent application 09/321,565 which is now U.S. Patent No. 6,221,682.---

Please replace the paragraph beginning at line 9 of page 17 with the following rewritten paragraph:

---In Figure 3 there is shown placement of a die (14) on a device (22) which may optionally be either a test device or an end use device. In either case the connections between pads (12) and

the pads (28) are the same. The wire connections (26) are completed after the die, as shown in Figure 1, is completely manufactured with discrete conductors already formed on the die (14). In the embodiment where device (22) is the end use device, the die will be first be KGD tested after forming metallurgical contacts between the stress tolerant solder ball array or flip-chip C4 array balls as illustrated in Figure 2. After KGD testing, the die (14) is removed from the test device (20) by melting the solder balls and separating the KGD from the device (20). Then, the die is installed in an end use device, as shown in Figure 3 by completion of a wire connections (26) between die (14) and end use device (22). In this embodiment, the stress tolerant solder ball connections to the test device provide an improved KGD test.---

Please replace the paragraph beginning at line 10 of page 18 with the following rewritten paragraph:

---An exemplary die is shown the photographs of Figure 4 and 5 which can be alternatively used to test the die as a known good die either by a wire bond test described with respect Figure 3, or by a stress tolerant solder ball or flip-chip C4 array bond test as shown and described in Figure 2. Figure 5 is a photograph showing the actual ball and pad structure. Figure 6 shows the pads (12) and the balls (10) on the same planar surface of a wafer (32).---

Please replace the paragraph beginning at line 19 of page 19 with the following rewritten paragraph:

---In Figure 6 there is shown a segment of a wafer (32) having wire bond pads along the right and left hand edges. In the center of wafer (32) is a cluster of solder balls (10) which are laid out in a square grid surrounding a neutral point (18) of the wafer segment (32). The ball grid may be any size and its size depends only upon the number of connections required and the limitation of a number of connections imposed by spacing from the center (18). Shown on the wafer are a plurality of chips (34) which are interconnected into a multi chip module all on the surface of wafer segment (32). Testing of the wafer segment (32) is either by use of a stress tolerant solder ball array (10), or by use of wire bond pads (12) as described with respect to the embodiments above relating to single known good die production. Although wafer segment (32) contains the plurality of integrated circuits (34), it clearly is definable as an integrated circuit merely having sub-integrated circuits (34) all connected together on the surface of wafer (32).---

IN THE CLAIMS:

Please amend claim 1 as follows:

1. A known good integrated circuit device having optional solder ball array or wire bond connections:

solder ball array connections on an integrated circuit device surface;

an array of wire bond connections electrically connected to the solder ball array connections;

wherein known good integrated circuit device testing is completed prior to mounting the integrated circuit device on an end use device by connecting a test device by wire bond connections or by solder ball connections; and

wherein when either the wire bond connections are used or the solder ball connections are used for known good integrated circuit device testing, the other is available for connection to an end use device.

Please cancel claims 11 - 43.

IN THE DRAWINGS:

Please make the changes marked in red on the sheets of drawings attached to the accompanying Letter to the Official Draftsperson.

REMARKS

This amendment cancels the claims in Group II (claims 11 - 43). Applicant now wishes to prosecute Group I (claims 1 - 10)

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Marking to Show Changes Made."**

It is submitted that the present amendment places the application in good form for allowance, and an early and favorable action for this application is respectfully solicited.

Respectfully submitted,

Ronald R. Snider
Reg. No. 24,962

Date: April 12, 2001

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RRS/bam

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

A new paragraph has been inserted at line 3 of page 1.

Paragraph beginning at line 9 of page 17 has been amended as follows:

In Figure 3 there is shown placement of a die (14) on a device (22) which may optionally be either a test device or an end use device. In either case the connections between pads **[(22)]** (12) and the pads (28) are the same. The wire connections (26) are completed after the die, as shown in Figure 1, is completely manufactured with discrete conductors already formed on the die (14). In the embodiment where device (22) is the end use device, the die will be first be KGD tested after forming metallurgical contacts between the stress tolerant solder ball array or flip-chip C4 array balls as illustrated in Figure 2. After KGD testing, the die (14) is removed from the test device (20) by melting the solder balls and separating the KGD from the device (20). Then, the die is installed in an end use device, as shown in Figure 3 by completion of a wire connections (26) between die (14) and end use device (22). In this embodiment, the stress tolerant solder ball connections to the test device provide an improved KGD test.

Paragraph beginning at line 10 of page 18 has been amended as follows:

An exemplary die is shown the photographs of Figure 4 and 5 which can be alternatively used to test the die as a known good die either by a wire bond test described with respect Figure 3, or by a stress tolerant solder ball or flip-chip C4 array bond test as shown and described in Figure 2. **[Figures 5 and 6 show]** Figure 5 is a photograph showing the actual ball and pad structure. Figure 6 shows the pads **[(28)]** (12) and the balls (10) on the same planar surface of **[the die (14)]** a wafer (32).

Paragraph beginning at line 19 of page 19 has been amended as follows:

In Figure 6 there is shown a segment of a wafer (32) having wire bond pads along the right and left hand edges. In the center of wafer (32) is a cluster of solder balls **[(16)]** (10) which are laid out in a square grid surrounding a neutral point (18) of the wafer segment (32). The ball grid may be any size and its size depends only upon the number of connections required and the limitation of a number of connections imposed by spacing from the center (18). Shown on the wafer are a plurality of chips (34) which are interconnected into a multi chip module all on the surface of wafer segment (32). Testing of the wafer segment (32) is either by use of a stress tolerant solder ball array (10), or by use of wire bond pads (12) as described with respect to the embodiments above relating to single known good die production.

Although wafer segment (32) contains the plurality of integrated circuits (34), it clearly is definable as an integrated circuit merely having sub-integrated circuits (34) all connected together on the surface of wafer (32).

In the Claims:

Claim 1 has been amended as follows:

1. A known good integrated circuit **[having]** device having optional solder ball array or wire bond connections:

solder ball array connections on an integrated circuit device surface;

an array of wire bond connections electrically connected to the solder ball array connections;

wherein known good integrated circuit device testing is completed prior to mounting the integrated circuit device on an end use device by connecting a test device by wire bond connections or by solder ball connections; and

wherein when either the wire bond connections are used or the solder ball connections are used for known good integrated circuit device testing, the other is available for connection to an end use device.

Claims 11 - 43 have been canceled.

S/N: TBA   4/12/2001   DOCKET NO.: L/M-102-DIV

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LETTER TO OFFICIAL DRAFTSPERSON

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

Attached are 2 sheets of drawings to be corrected as shown in red.

Respectfully submitted,

Ronald R. Snider
Reg. No. 24,962

Date: April 12, 2001

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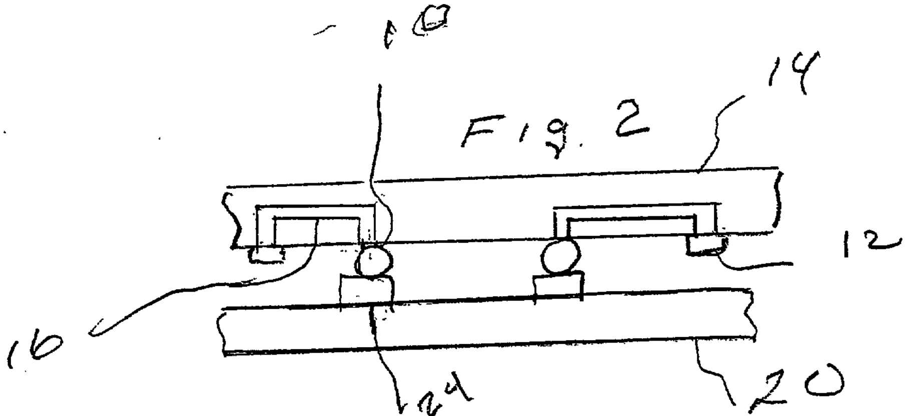

Fig. 2

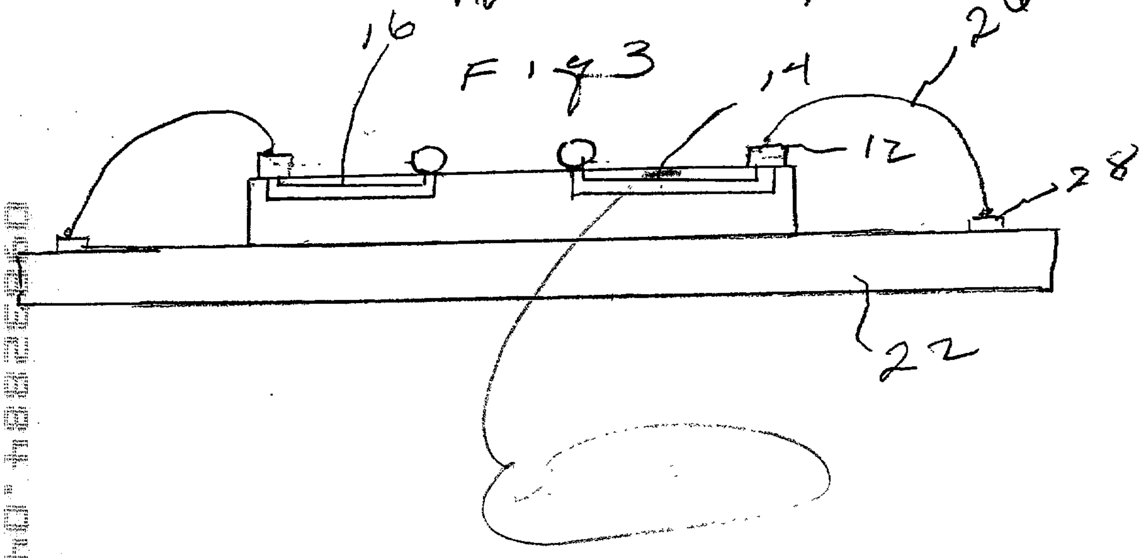

Fig. 3

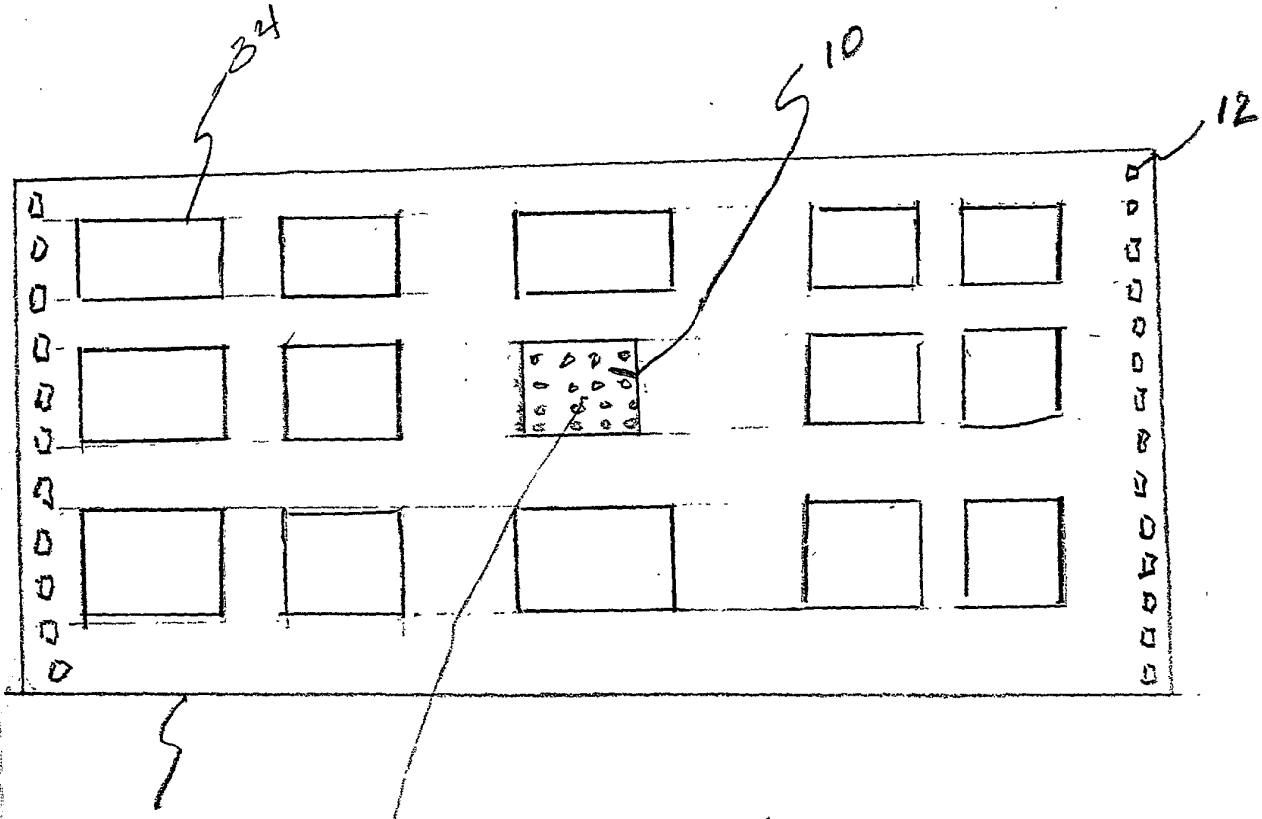

FIGURE 6